

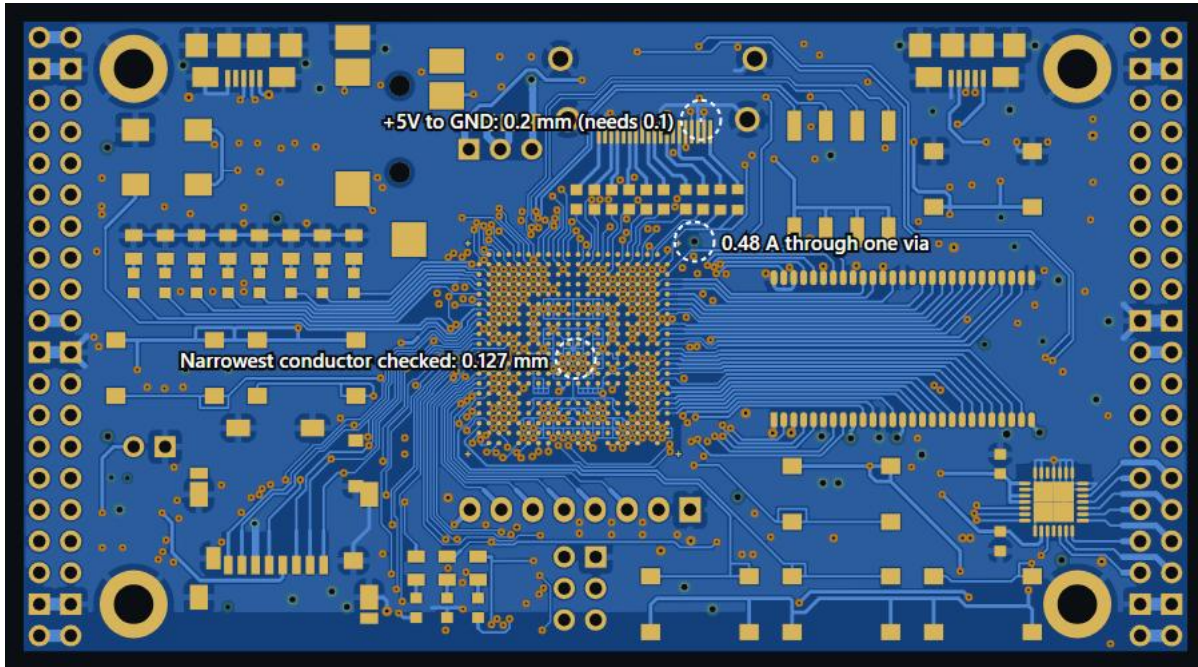
# ULX3S 3V3 rail readiness report

Pass qualification before you build

Schema

bcert-report/1

**Fix before you build** 5 pass, 1 with one change, 1 failing, 1 not assessed, 3 coming



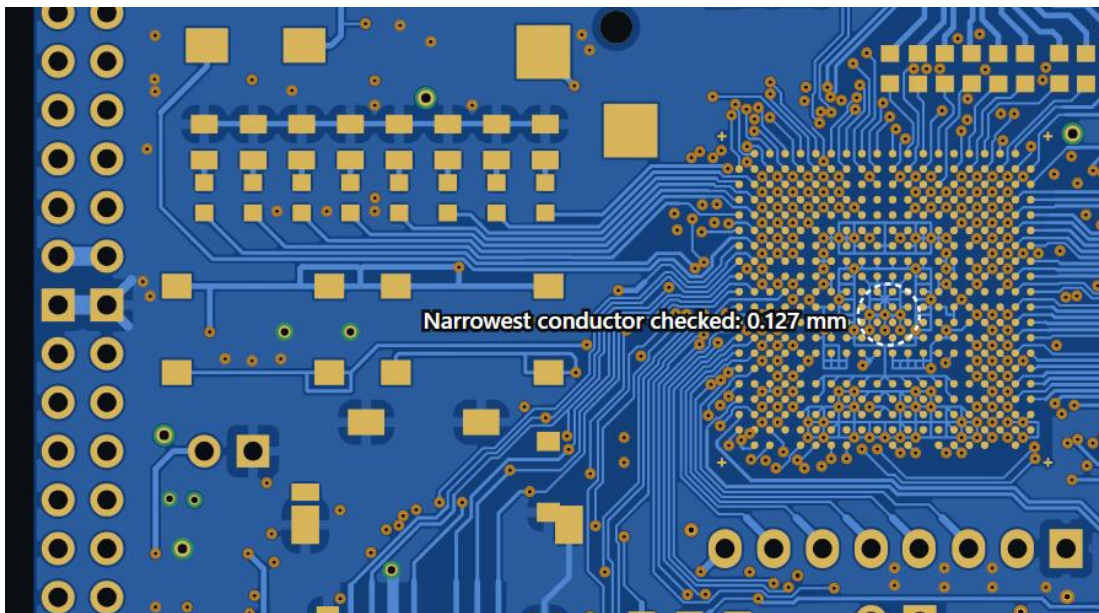
Top copper: every via ringed green (keeps its Class 3 ring) or amber (widen this pad), with the spacing and ampacity checks marked.

## UL 796 construction - Pass

UL 796. meets the fab's UL-recognized construction

| ULX3S on JLCPCB meets the fab's UL-recognized construction (UL 796 design check).

|                    |        |
|--------------------|--------|
| Fab                | JLCPCB |
| Conductors checked | 4811   |
| Findings           | 0      |
| Board thickness    | 1.6 mm |



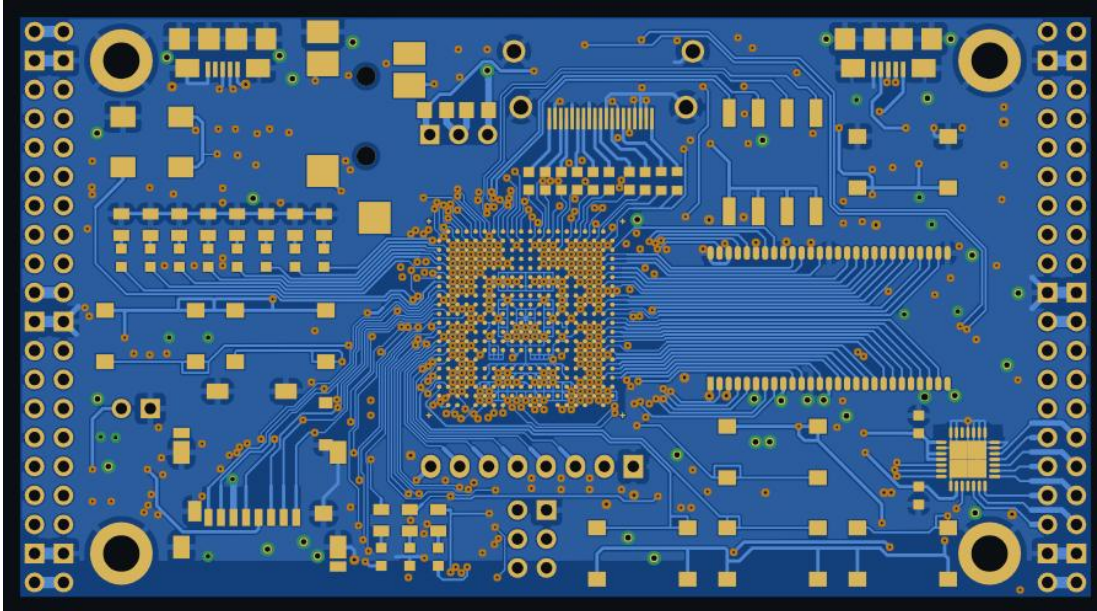
| Method: Construction rules checked against the fab's published UL 796 capabilities

## IPC-6012 Class 2 - Pass

IPC-6012 Class 2. Class 2: 100% via ring retention under the fab drill tolerance

| ULX3S is IPC-6012 Class 2 ready (100% via ring retention under the fab's drill tolerance).

Vias 554  
Ring retention 100%  
Nominal rings Pass  
Aspect ratio (max) 7.9  
Monte Carlo boards 1000



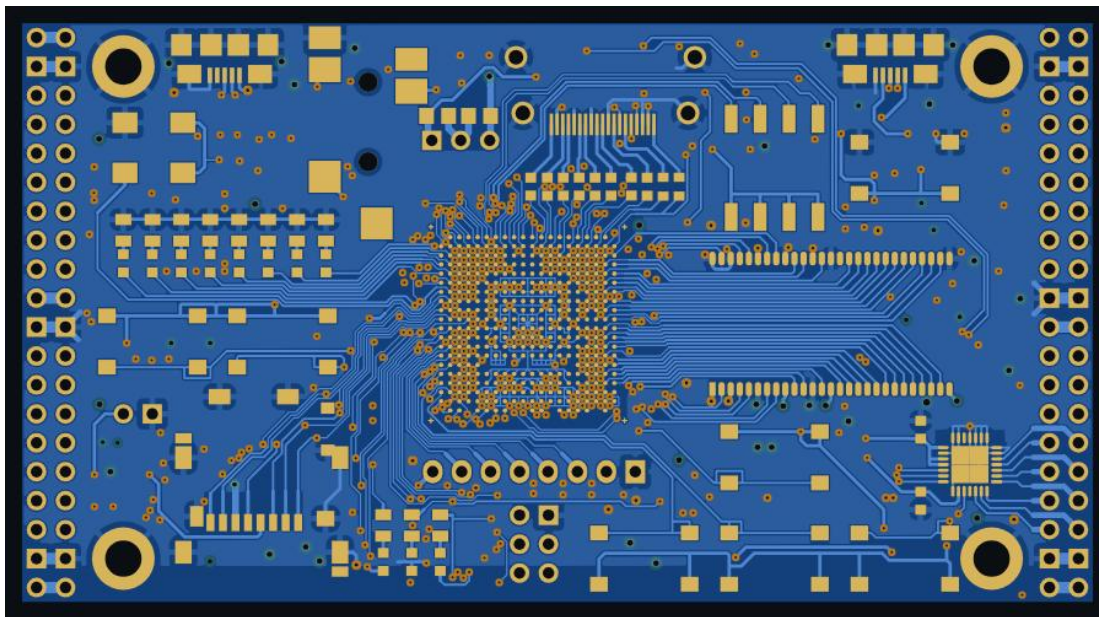
| Method: Monte Carlo of every via over the fab drill and layer-registration tolerance

## IPC-6012 Class 3 - One change

IPC-6012 Class 3. Class 3: 77.9% ring retention as drawn, 100% with the pad change

Vias 554  
Ring retention 77.9%  
Nominal rings Pass  
Aspect ratio (max) 7.9  
Monte Carlo boards 1000  
Ring retention with the change 100%

| Finding                              | At            | The one change        |
|--------------------------------------|---------------|-----------------------|
| 488 vias: drill 0.2 mm, pad 0.419 mm | 114.8, -74.37 | Pad 0.419 to 0.55 mm  |
| 13 vias: drill 0.3 mm, pad 0.6 mm    | -             | Pad 0.6 to 0.65 mm    |
| 3 vias: drill 0.254 mm, pad 0.5 mm   | -             | Pad 0.5 to 0.604 mm   |
| 5 vias: drill 0.25 mm, pad 0.5 mm    | -             | Pad 0.5 to 0.6 mm     |
| 1 vias: drill 0.254 mm, pad 0.454 mm | -             | Pad 0.454 to 0.604 mm |



### As drawn

0.419 mm pad

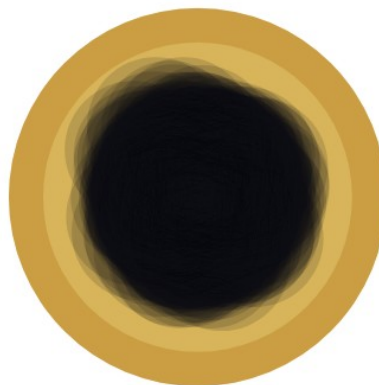


**75.2% keep the ring**

102 of 400 hits in the band  
2 break out of the pad

### With the change

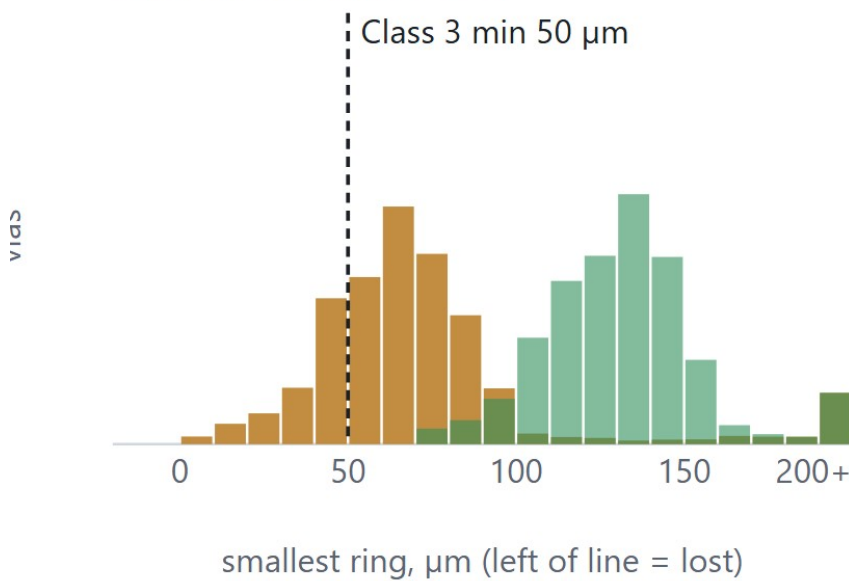
0.55 mm pad



**100% keep the ring**

0 of 400 hits in the band  
0 break out of the pad

**As drawn: 77.9% keep the ring**  
**With the change: 100%**

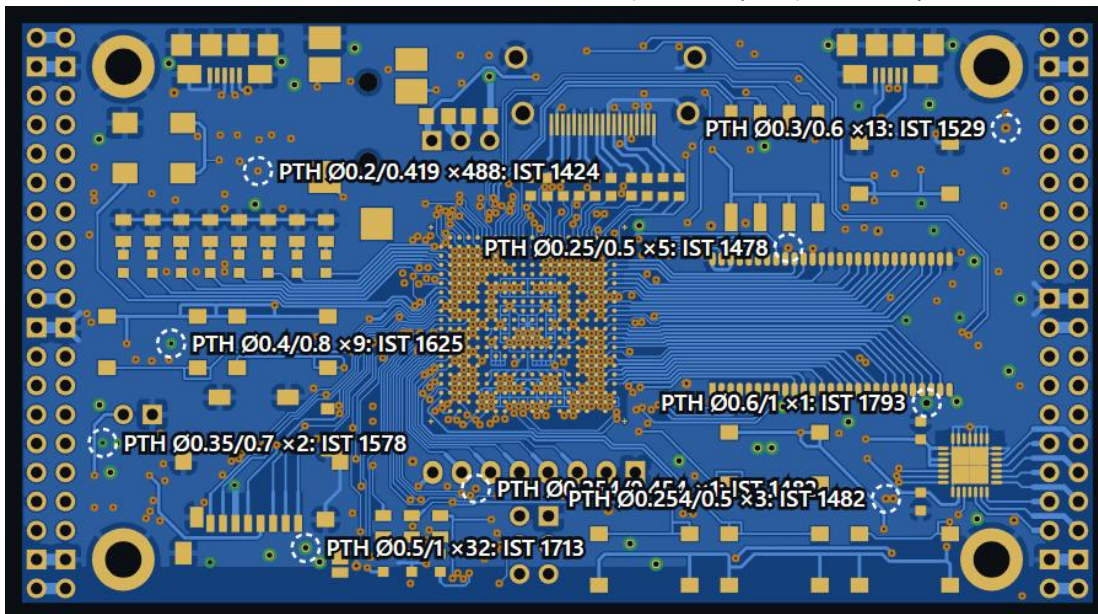


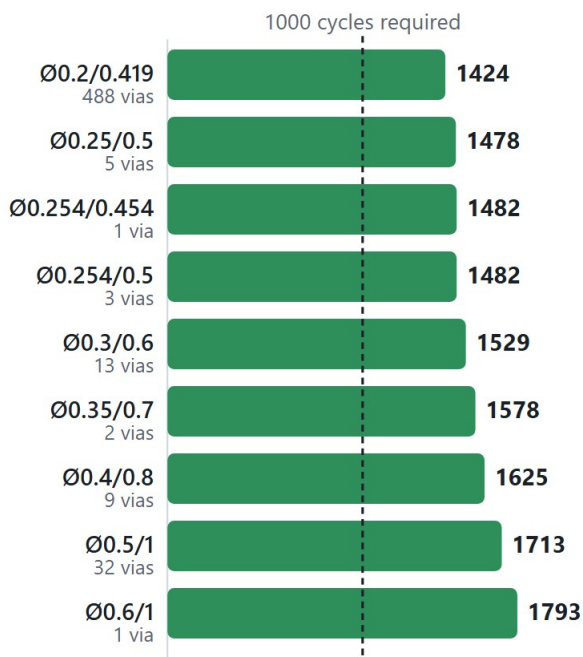
| Method: Monte Carlo of every via over the fab drill and layer-registration tolerance

#### Coupon predictions - Pass

IPC-6012 coupons. 9 via structures predicted to pass solder float, 6x reflow and IST; fewest IST cycles 1424 against 1000 required

|                                          |                                          |
|------------------------------------------|------------------------------------------|
| PTH $\emptyset 0.2/0.419$ F.Cu?B.Cu x488 | IST 1424 / 1000, float pass, reflow pass |
| PTH $\emptyset 0.25/0.5$ F.Cu?B.Cu x5    | IST 1478 / 1000, float pass, reflow pass |
| PTH $\emptyset 0.254/0.454$ F.Cu?B.Cu x1 | IST 1482 / 1000, float pass, reflow pass |
| PTH $\emptyset 0.254/0.5$ F.Cu?B.Cu x3   | IST 1482 / 1000, float pass, reflow pass |
| PTH $\emptyset 0.3/0.6$ F.Cu?B.Cu x13    | IST 1529 / 1000, float pass, reflow pass |
| PTH $\emptyset 0.35/0.7$ F.Cu?B.Cu x2    | IST 1578 / 1000, float pass, reflow pass |





| Method: Plated-via fatigue model for each via structure

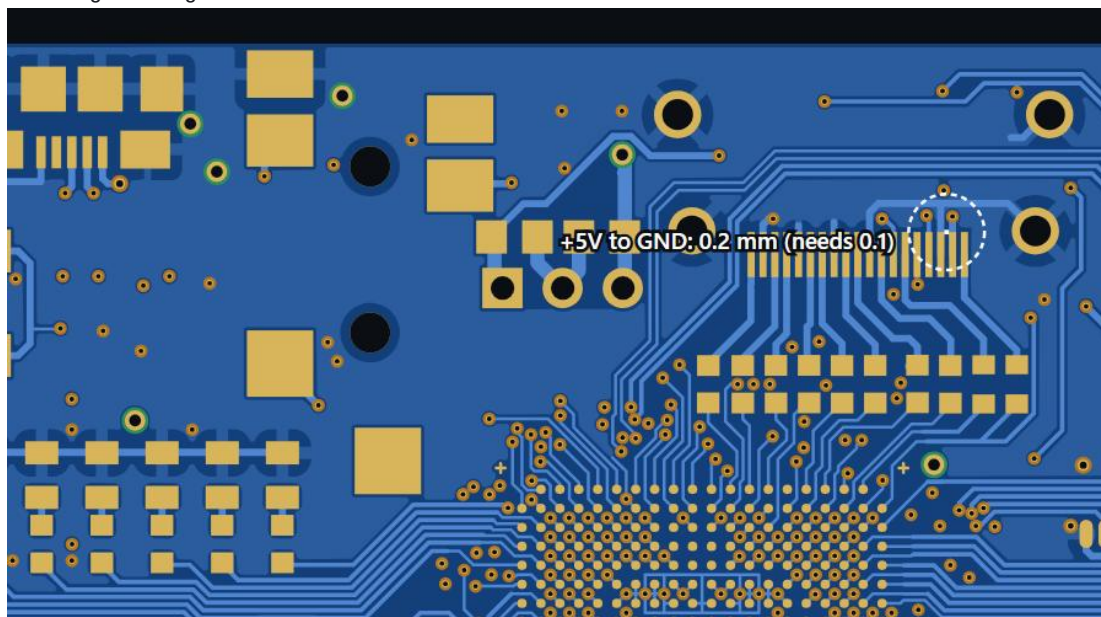
### Creepage and clearance - Pass

IPC-2221 spacing. +5V to GND: clearance 0.2 mm, 0.1 mm required

Clearance 0.2 mm (need 0.1)

Surface path 0.2 mm

Working voltage 5 Vrms



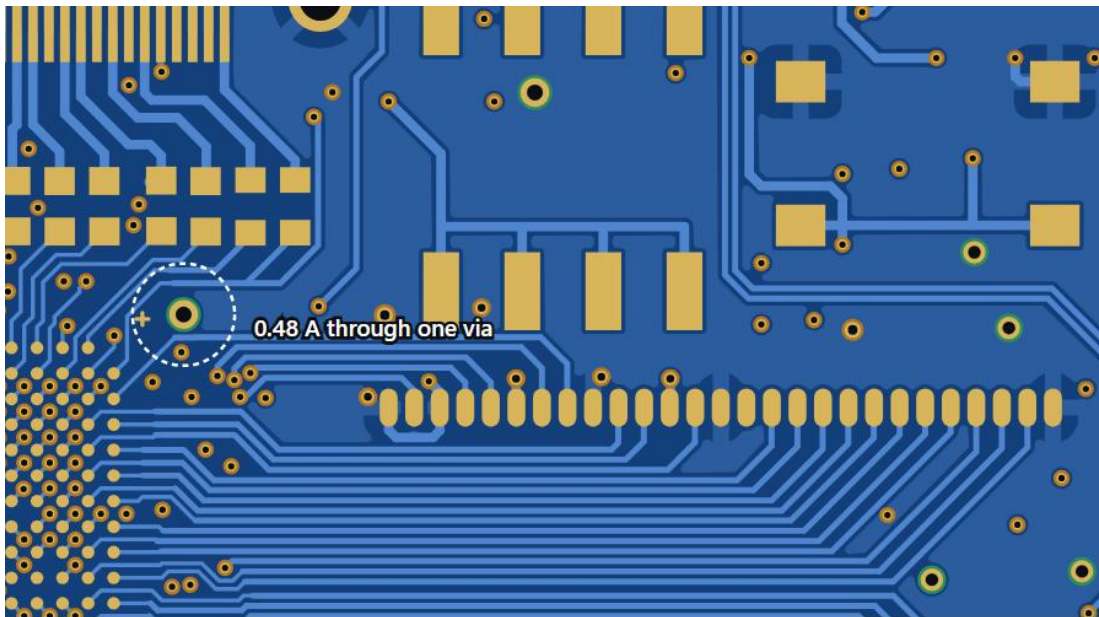
| Method: Shortest air and surface paths between the nets

### Trace ampacity - Pass

IPC-2221 / IPC-2152 ampacity. vccio33 0.48 A: pass; core1v1 0.3 A: pass

vccio33 (+3V3) Peak current density, B.Cu 20.48 of 68.33 A/mm<sup>2</sup>; Busiest via current 0.48 of 1.25 A; Trace rise 0.02 of 10 K

core1v1 (+1V1) Peak current density, In1.Cu 14.29 of 34.17 A/mm<sup>2</sup>; Busiest via current 0.3 of 1.25 A; Trace rise 0.03 of 10 K



| Method: Current capacity per rail from the IPC-2221 / IPC-2152 charts

## Vibration and drop - Fails

Steinberg vibration fatigue / JESD22-B111 board-level drop. Steinberg: all 7 assessed parts within their allowable deflection, lowest margin 5.62x (U1); JESD22-B111 drop: U1 1927 microstrain over the 1500 microstrain limit

|                        |                                                                            |
|------------------------|----------------------------------------------------------------------------|
| First mode             | 1265 Hz, board edges simply supported                                      |
| Random input           | 8.9 Grms, flat 0.04 g <sup>2</sup> /Hz from 20 to 2000 Hz                  |
| Drop input             | 1500 g, 0.5 ms half-sine (condition B)                                     |
| U1 BGA 18 x 18 mm      | vibration 0.040 of 0.224 mm (5.62x); drop 1927 of 1500 microstrain (0.78x) |
| U2 QFP 22.1 x 10.16 mm | vibration 0.028 of 0.507 mm (18x); drop 1345 of 1500 microstrain (1.12x)   |
| U8 LCC 5 x 5 mm        | vibration 0.010 of 0.658 mm (68x); drop 465 of 1500 microstrain (3.23x)    |
| U7 QFP 4.9 x 3.9 mm    | vibration 0.017 of 1.495 mm (86x); drop 836 of 1500 microstrain (1.79x)    |
| U10 QFP 4.9 x 3.9 mm   | vibration 0.026 of 1.157 mm (45x); drop 1252 of 1500 microstrain (1.2x)    |
| U6 LCC 4 x 4 mm        | vibration 0.013 of 0.735 mm (56x); drop 635 of 1500 microstrain (2.36x)    |
| U9 LCC 31.4 x 18 mm    | vibration 0.016 of 0.142 mm (9.12x); drop 752 of 1500 microstrain (1.99x)  |

| Finding                                                                                                      | At | The one change |
|--------------------------------------------------------------------------------------------------------------|----|----------------|
| U1 (BGA) sees 1927 microstrain at the board surface in the condition B drop, over the 1500 microstrain limit | -  | -              |

| Method: Plate model of the board with edges simply supported, 7 IC bodies from the KiCad placement; Steinberg allowable deflection  $Z = 0.00022 B / (C h r \sqrt{L})$  against the 3-sigma deflection at each part; drop as the modal response to the half-sine. Part masses and the corner mounting holes are not modelled, and both raise deflection and strain

## Solder joint fatigue - Not assessed

IPC-9701 solder joint thermal-cycle fatigue. Not assessed: no cycles-to-failure is given for any part. This report has no solder-joint life model and no sourced package or laminate CTE to run one on, and it does not invent them

|                           |                                                                              |
|---------------------------|------------------------------------------------------------------------------|
| Profile to assess against | IPC-9701 TC1, 0 to 100 C (an input of this report)                           |
| BGA joints                | U1 LFE5U-85F-6BG381C, 381 balls at 0.8 mm pitch, 18 x 18 mm body             |
| Leaded joints             | U2, U7, U10                                                                  |
| Leadless joints           | U8, U6, U9                                                                   |
| Missing inputs            | solder-joint life model; package and laminate in-plane CTE; U1 ball standoff |

| Method: Parts taken from the KiCad placement (7 IC bodies). The ball-map adapter exists for flip-chip BGA builds; the Engelmaier life equation it feeds is not in the tree, so no part is assessed

### **Reflow warpage - Coming**

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IPC-TM-650 warpage. Coming next

### **Conductive anodic filament - Coming**

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IPC-TM-650 CAF. Coming next

### **FCC pre-compliance - Coming**

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FCC 47 CFR 15.109. Coming next